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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/822,971

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Bahareh Ghaffari

COS-002

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7590 03/13/2007  
William L. Botjer  
P.O. Box 478  
Center Moriches, NY 11934

EXAMINER

STIGLIC, RYAN M

ART UNIT

PAPER NUMBER

2111

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

03/13/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/822,971

Applicant(s)

GHAFFARI ET AL.

Examiner

Ryan M. Stiglic

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-17 is/are allowed.
- 6) ☒ Claim(s) 1-4, 14 and 18 is/are rejected.
- 7) ☒ Claim(s) 5-13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. Claims 1-18 are pending and have been examined.
2. Claims 1-4, 14 and 18 are rejected.
3. Claims 5-13 are objected to.
4. Claims 15-17 are allowed.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujimoto et al. (US Patent No. 6,385,681).

For claim 1 Fujimoto discloses:

An interconnecting unit for coupling a plurality of hosts to a plurality of storage devices, the coupling involving exchange of a plurality of serial I/O structures between the plurality of hosts and the plurality of storage devices, the interconnecting unit comprising:

- a. a plurality of device control units enabling distribution of a plurality of commands to the plurality of storage devices, each of the plurality of commands being an element of a serial I/O structure (Fig. 1 & 4, 104; col. 5, ll. 9-23; col. 7, line 60 – col. 8, line 10; The

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control units are used to control the distribution of access requests sent from a host computer.);

b. a plurality of host interface units, each of the plurality of host interface units synchronizing data between a host and the interconnecting unit (Fig. 1, 102; col. 5, ll. 9-10; col. 9, ll. 11-16; The host interface units receive information from the host computer and synchronize the data for transport through the disk array controller.);

c. a plurality of device interface units, each of the plurality of device interface units synchronizing data between a storage device and the interconnecting unit (Fig. 1, 130; col. 5, ll. 24-25; col. 9, ll. 11-16; The disk interface units receive/transmit data to the disk drives synchronized for transmission through the disk array controller.); and

d. an interconnect routing unit to connect a device control unit to a device interface unit (Fig. 1 & 6, 13; col. 8, ll. 11-44; The selector units control routing of information through the disk array controller.).

For claim 2 Fujimoto discloses:

The interconnecting unit according to claim 1, wherein each of the plurality of the elements of a serial I/O structure is transmitted in a serial bit format (col. 13, ll. 1-17; Fujimoto discloses the use of Fibre Channels to transmit data. High-speed Fibre Channels transmit data in a serial bit format.).

For claim 3 Fujimoto discloses:

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The interconnecting unit according to claim 1, wherein each of the plurality of host interface units converts each of the plurality of the received elements of the serial I/O structure in a serial bit stream format to a character bit format (col. 13, ll. 1-17; Fujimoto discloses the use of Fibre Channels to transmit data. Fibre Channel communication utilizes 8B/10B encoding thus meeting the claim limitations.).

For claim 4 Fujimoto discloses:

The interconnecting unit according to claim 1, wherein each of the plurality of device interface units converts each of the plurality of the received elements of the serial I/O structure in a serial bit stream format to a character bit format (col. 13, ll. 1-17; Fujimoto discloses the use of Fibre Channels to transmit data. Fibre Channel communication utilizes 8B/10B encoding thus meeting the claim limitations.).

7. Claims 1-4, 14 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsunami et al. (US Patent Application Publication No. US 2002/0095549).

For claim 1 Matsunami discloses:

An interconnecting unit for coupling a plurality of hosts to a plurality of storage devices, the coupling involving exchange of a plurality of serial I/O structures between the plurality of hosts and the plurality of storage devices, the interconnecting unit comprising:

- a. a plurality of device control units enabling distribution of a plurality of commands to the plurality of storage devices, each of the plurality of commands being an element of a

serial I/O structure (Fig. 5, 2022; [0061-0064]; The Switching Controller manages the distribution of information to the storage units.);

- b. a plurality of host interface units, each of the plurality of host interface units synchronizing data between a host and the interconnecting unit (Fig. 3, 203; more specifically Fig. 5, 2023; The Interface controller provides an interface to the plurality of host units.);
- c. a plurality of device interface units, each of the plurality of device interface units synchronizing data between a storage device and the interconnecting unit (Fig. 3, 202; [0042,0044]; The disk array node interfaces 202 provide a connection between the disk drives and the disk array switch.); and
- d. an interconnect routing unit to connect a device control unit to a device interface unit (Fig. 3-4, 201; [0042-0043]; The crossbar switch provides routing from host to disk drive devices.).

For claim 2 Matsunami discloses:

The interconnecting unit according to claim 1, wherein each of the plurality of the elements of a serial I/O structure is transmitted in a serial bit format ([0085]; Matsunami discloses the use of Fibre Channels to transmit data. High-speed Fibre Channels transmit data in a serial bit format.).

For claim 3 Matsunami discloses:

The interconnecting unit according to claim 1, wherein each of the plurality of host interface units converts each of the plurality of the received elements of the serial I/O structure in a serial

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bit stream format to a character bit format ([0085]; Matsunami discloses the use of Fibre Channels to transmit data. Fibre Channel communication utilizes 8B/10B encoding thus meeting the claim limitations.).

For claim 4 Matsunami discloses:

The interconnecting unit according to claim 1, wherein each of the plurality of device interface units converts each of the plurality of the received elements of the serial I/O structure in a serial bit stream format to a character bit format ([0085]; Matsunami discloses the use of Fibre Channels to transmit data. Fibre Channel communication utilizes 8B/10B encoding thus meeting the claim limitations.).

For claim 14 Matsunami discloses:

A data storage system, the data storage system comprising:

- a. a plurality of hosts, each of the plurality of hosts being queue capable (Fig. 1, 30; [0085-0086]; The hosts use a serial SCSI over fibre channel protocol, which is a queue capable protocol.);
- b. a plurality of storage devices (Fig. 2, 104);
- c. an interconnecting unit for coupling the plurality of hosts to the plurality of storage devices, the coupling involving exchange of a plurality of serial I/O structure between the plurality of hosts and the plurality of storage devices, the interconnecting unit comprising:

- i. a plurality of device control units enabling distribution of a plurality of commands to the plurality of storage devices, each of the plurality of commands being an element of serial I/O structure (Fig. 5, 2022; [0061-0064]; The Switching Controller manages the distribution of information to the storage units.);
- ii. a plurality of host interface units, each of the plurality of host interface units synchronizing the data between the host and the interconnecting unit, each of the plurality of host interface units converting the elements of the serial I/O structure in a serial bit stream format to a character bit format (Fig. 3, 203; more specifically Fig. 5, 2023; The Interface controller provides an interface to the plurality of host units.;[0085]; Matsunami discloses the use of Fibre Channels to transmit data. Fibre Channel communication utilizes 8B/10B encoding thus meeting the claim limitations.);
- iii. a plurality of device interface units, each of the plurality of device interface units synchronizing the data between the storage device and the interconnecting unit, the device interface unit converting the element of the serial I/O structure in the serial bit stream format to the character bit format (Fig. 3, 202; [0042,0044]; The disk array node interfaces 202 provide a connection between the disk drives and the disk array switch.;[0085]; Matsunami discloses the use of Fibre Channels to transmit data. Fibre Channel communication utilizes 8B/10B encoding thus meeting the claim limitations.); and



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- iv. an interconnect routing unit to connect a device control unit to a device interface unit (Fig. 3-4, 201; [0042-0043]; The crossbar switch provides routing from host to disk drive devices.).

For claim 18 Matsunami discloses:

The method according to claim 14, wherein the step of locking comprises the steps of:

- a. identifying whether the operation is a read operation or a write operation ([0060]);
- b. the storage device sending a read data to the host if the read operation is to be performed (Fig. 10, e; [0066]); and
- c. the storage device sending a response to the host enabling the host to write a data if the write operation is to be performed (Fig. 19, g1; [0102]).

*Allowable Subject Matter*

8. Claims 5-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Claims 15-17 are considered allowable over the prior art of record. The Examiner has done a thorough search and found no prior art of record, alone or in combination, that teaches or fairly suggests the combination of limitations presented in independent claim 15. Fujimoto and Matsunami (discussed above) are each drawn to an interconnecting unit for providing routing of serial I/O structures to a plurality of disk drives. Each of the interconnecting units, receives

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commands from a host, delivers the received command to the proper target and receives responses from the identified targets in the situation where no error is encountered. The interconnecting units are further configured to route the responses to the appropriate host device such that the transaction may be completed. The Examiner however, was unable to find prior art that suitably taught or suggested (f) identifying whether the storage device is queue capable; (h) locking host and the responding device for operation, the operation being based on the command; and (i) checking if there is a command in a queue taken in combination with the other recited claim limitations. As such, claims 15-17 are considered allowable over the prior art of record.

### *Conclusion*

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure because it relates to storage systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



RMS

PAUL R. MYERS  
PRIMARY EXAMINER